

WHAT IS CLAIMED IS:

1 1. A method of forming a semiconductor non-volatile memory cell,
2 comprising:
3 forming a first insulating layer over a substrate region;
4 forming a first doped polysilicon layer over the first insulating layer;
5 forming a first undoped polysilicon layer over and in contact with the first
6 doped polysilicon layer, the first doped and first undoped polysilicon layers forming a
7 floating gate;
8 forming a second insulating layer over and in contact with the first undoped
9 polysilicon layer;
10 forming a second undoped polysilicon layer over and in contact with the
11 second insulating layer; and
12 forming a second doped polysilicon layer over and in contact with the second
13 undoped polysilicon layer, the second doped and undoped polysilicon layers forming a
14 control gate.

1 2. The method of claim 1 further comprising:
2 before said first doped polysilicon forming act, forming a third undoped
3 polysilicon layer over and in contact with the first insulating layer wherein the first doped
4 polysilicon layer overlies and is in contact with the third undoped polysilicon layer, the third
5 undoped polysilicon layer forming part of the floating gate.

1 3. The method of claim 1 wherein the first insulating layer is a tunnel
2 oxide layer and the second insulating layer is one of composite oxide-nitride-oxide dielectric
3 layer and composite oxide-nitride-oxide-nitride dielectric layer .

1 4. The method of claim 1 wherein a thickness of each doped polysilicon
2 layer is greater than a thickness of a corresponding undoped polysilicon layer by a factor in
3 the range of two to four.

1 5. The method of claim 1 further comprising:
2 forming insulating spacers along sidewalls of the stack made up of the first
3 insulating layer, the floating gate, the second insulating layer, and the control gate; and
4 forming source and drain regions in the substrate.

1 6. The method of claim 1 wherein each of said first and second doped
2 polysilicon layers forming acts comprises depositing an in-situ doped polysilicon layer.

1 7. The method of claim 1 wherein the memory cell is any one of a
2 stacked-gate non-volatile cell and a split gate non-volatile cell.

1 8. The method of claim 1 wherein each of the first and second doped
2 polysilicon layers has a doping concentration and a thickness greater than a thickness of the
3 corresponding first and second undoped polysilicon layers so as to prevent polysilicon
4 depletion in each of the floating gate and the control gate.

1 9. The method of claim 1 wherein the non-volatile memory cell is any
2 one of ROM, flash EPROM, and EEPROM.

1 10. A method of forming a semiconductor transistor, comprising:
2 forming an insulating layer over a substrate region;
3 forming an undoped polysilicon layer over and in contact with the insulating
4 layer; and
5 forming a doped polysilicon layer over and in contact with the undoped
6 polysilicon layer, the doped and undoped polysilicon layers forming a gate of the transistor.

1 11. The method of claim 10 wherein the insulating layer is a gate oxide
2 layer.

1 12. The method of claim 10 wherein a thickness of the doped polysilicon
2 layer is greater than a thickness of the undoped polysilicon layer by a factor in the range of
3 two to four.

1 13. The method of claim 10 further comprising:
2 forming insulating spacers along sidewalls of the gate; and
3 forming source and drain regions in the substrate.

1 14. The method of claim 10 wherein said doped polysilicon layer forming
2 act comprises depositing an in-situ doped polysilicon layer.

1 15. The method of claim 10 wherein the transistor is any one of a NMOS
2 transistor, PMOS transistor, enhancement transistor, and depletion transistor.

1 16. The method of claim 10 wherein the doped polysilicon layer has a
2 doping concentration and a thickness greater than a thickness of the undoped polysilicon
3 layer so as to prevent polysilicon depletion in the gate.

1 17. A semiconductor non-volatile memory cell comprising:
2 a first insulating layer over a substrate region;
3 a first doped polysilicon layer over the first insulating layer;
4 a first undoped polysilicon layer over and in contact with the first doped
5 polysilicon layer, the first doped and first undoped polysilicon layers forming a floating gate;
6 a second insulating layer over and in contact with the first undoped polysilicon
7 layer;
8 a second updoped polysilicon layer over and in contact with the second
9 insulating layer; and
10 a second doped polysilicon layer over and in contact with the second undoped
11 polysilicon layer, the second doped and undoped polysilicon layers forming a control gate.

1 18. The memory cell of claim 17 further comprising a third undoped
2 polysilicon layer over and in contact with the first insulating layer wherein the first doped
3 polysilicon layer overlies and is in contact with the third undoped polysilicon layer, the third
4 undoped polysilicon layer forming part of the floating gate.

1 19. The memory cell of claim 17 wherein the first insulating layer is a
2 tunnel oxide layer and the second insulting layer is one of a composite oxide-nitride-oxide
3 dielectric layer and a composite oxide-nitride-oxide-nitride dielectric layer.

1 20. The memory cell of claim 17 wherein a thickness of each doped
2 polysilicon layer is greater than a thickness of a corresponding undoped polysilicon layer by a
3 factor in the range of two to four.

1 21. The memory cell of claim 17 further comprising:
2 insulating spacers along sidewalls of the stack made up of the first insulting
3 layer, the floating gate, the second insulating layer, and the control gate; and
4 source and drain regions in the substrate.

1 22. The memory cell of claim 17 wherein each of said first and second
2 doped polysilicon layers comprises are in-situ doped with impurities.

1 23. The memory cell of claim 17 wherein the memory cell is any one of a
2 stacked-gate cell and split gate cell.

1 24. The memory cell of claim 17 wherein each of the first and second
2 doped polysilicon layers has a doping concentration and a thickness greater than a thickness
3 of the corresponding first and second undoped polysilicon layers so as to prevent polysilicon
4 depletion in each of the floating gate and the control gate.

1 25. The memory cell of claim 17 wherein the non-volatile memory cell is
2 any one of ROM, flash EPROM, and EEPROM.

1 26. A semiconductor transistor comprising:
2 an insulating layer over a substrate region;
3 an undoped polysilicon layer over and in contact with the insulating layer; and
4 a doped polysilicon layer over and in contact with the undoped polysilicon
5 layer, the doped and undoped polysilicon layers forming a gate of the transistor.

1 27. The transistor of claim 26 wherein the insulating layer is a gate oxide
2 layer.

1 28. The transistor of claim 26 wherein a thickness of the doped polysilicon
2 layer is greater than a thickness of the undoped polysilicon layer by a factor in the range of
3 two to four.

1 29. The transistor of claim 26 further comprising:
2 insulating spacers along sidewalls of the gate; and
3 source and drain regions in the substrate.

1 30. The transistor of claim 26 wherein the doped polysilicon layer is in-
2 situ doped with impurities.

1 31. The transistor of claim 26 wherein the transistor is any one of a NMOS
2 transistor, PMOS transistor, enhancement MOS transistor, and depletion MOS transistor.

1 32. The transistor of claim 26 wherein the doped polysilicon layer has a
2 doping concentration and a thickness greater than a thickness of the undoped polysilicon
3 layer so as to prevent polysilicon depletion in the gate.

1 33. A semiconductor structure comprising:
2 an undoped polysilicon layer;
3 a doped polysilicon layer in contact with the undoped polysilicon layer; and
4 an insulating layer in contact with the undoped polysilicon layer, wherein the
5 undoped polysilicon layer is sandwiched between the doped polysilicon layer and the
6 insulating layer.

1 34. The structure of claim 33 wherein a thickness of the doped polysilicon
2 layer is greater than a thickness of the undoped polysilicon layer by a factor in the range of
3 two to four.

1 35. The structure of claim 33 wherein the structure is one of a ROM cell, a
2 flash EPROM cell, an EEPROM cell, a DRAM cell, and a SRAM cell, a NMOS transistor, a
3 PMOS transistor, an enhancement MOS transistor, and a depletion MOS transistor.